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(54) **Semiconductor device.**

(57) A semiconductor device wherein barrier regions (23a, 23b) are formed on those portions of the surface of a semiconductor substrate (20) which lie below and around the expected connection area (22c) of a first wire (22) to which a second wire (24) is connected through a contact hole (26) with the opposite conductivity type to that of the semiconductor substrate (20).

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Semiconductor device

This invention relates to an improvement on a semiconductor device wherein one group of lattice-arranged wire layers formed on a semiconductor substrate intersects the other group.

Two wire layers included in a lattice arrangement which stepwise intersect each other, for example, at right angles generally have such a junction as shown in Fig. 1. Where a first wire layer 1 of polycrystalline silicon acting as a gate electrode is connected to a second rectangularly intersecting wire layer of aluminium at the junction, it is necessary to enlarge the contact section 4 of the first wire layer 1 or let said contact section 4 project from the first wire layer 1 in order to compensate for those changes in the position of a contact hole 3 produced by etching which might result from the displacement of a mask. Unless the contact section 4 is provided, the displacement of the mask would give rise to the possibility of the second wire layer 2 being short-circuited with a semiconductor substrate 5, in case, as shown in Fig. 2, the contact hole 3 is displaced from the end of the first wire layer 1. For the formation of such large contact section 4, therefore, the pitch of every adjacent first wire layers 1 can not be reduced, presenting great difficulties in elevating the density

with which the aforesaid lattice-arranged wire layers are integrated.

It is accordingly an object of this invention to provide a semiconductor device in which the pitch of every adjacent wires can be reduced and the wires can be integrated with a greater density.

Another object of the invention is to provide a highly reliable semiconductor device in which short-circuiting between the wires and semiconductor substrate can be completely suppressed.

To attain the above-mentioned object, this invention provides a semiconductor device in which those portions of the surface of a semiconductor substrate which are disposed below and around the that section of the first wire to which the second wire is to be connected is provided with a barrier region having the opposite conductivity type to that of the semiconductor substrate.

The barrier region prevents short circuiting between the semiconductor substrate and part of the second wire connected to the first wire, thereby eliminating the necessity of forming a large contact section as is the case with the prior art, and minimizing the wire pitch.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a plan view showing the manner in which the lattice-arranged wires of the prior art semiconductor device are connected to each other;

Fig. 2 is a sectional view showing short-circuiting between the semiconductor substrate and second wire occurring in the conventional semiconductor device;

Fig. 3 is a sectional view of a semiconductor device embodying this invention in which the construction of the junction of every adjacent wires is improved;

Fig. 4 is a plan view showing the junction of

every adjacent wires of the semiconductor device of the invention; and

Fig. 5 is a sectional view of the semiconductor device of the invention.

Description is now given with reference to Fig. 3 of a semiconductor device in which the construction of every adjacent wires is improved to prevent the short-circuiting between the semiconductor substrate and the second wire. A barrier region 13 is formed on that portion of the surface of the semiconductor substrate 10 which surrounds the expected connection area 12c of a first wire 12 with the opposite conductivity type to that of the semiconductor substrate 10 by ion implantation with a first insulation layer 11 and the first wire 12 formed thereon used as a mask. The second wire 14 is connected to the expected connection area 12c of the first wire 12 through a contact hole 16 of a second insulation layer 15. The second wire 14 separated from the semiconductor substrate 10 by a PN junction is prevented from short-circuiting with the semiconductor substrate 10.

However, the second wire 14 prepared from, for example, aluminium often intrudes during formation into the semiconductor substrate from a boundary between that portion of the first insulation layer 11 which lies under the expected connection area 12c of the first wire 12 and the barrier region 13. As a result, short-circuiting arises between the semiconductor substrate 10 and second wire 14, thereby reducing the reliability and yield of a semiconductor device produced.

With the semiconductor device of this invention shown in Figs. 4 and 5, it is possible to prevent short-circuiting between the semiconductor substrate 10 and second wire due to its intrusion into said semiconductor substrate 10. As shown in Fig. 5, barrier regions 23a, 23b are formed on those portions of the

surface of the semiconductor substrate 20 which lie around and below the expected connection area 22c of the first wire 22 deposited on the first insulation layer 21 with the opposite conductivity type to that of the semiconductor substrate 20. A contact hole 26 is formed in a second insulation layer 25 deposited on the first wire 22. A second wire 24 is connected to the expected connection area 22c, which has been exposed. The contact hole 26 may be larger than the expected connection area 22c, but should be smaller than the barrier regions 23a, 23b. As indicated in Figs. 4 and 5, the expected contact area 22c of the first wire 22 may be as wide as the first wire 22, thereby minimizing the interwire distance.

The semiconductor device of this invention can be manufactured by the same process as that by which a transistor is produced, without applying any additional step. Namely, the barrier regions can be formed by the steps of selectively depositing a resist on a silicon oxide layer already mounted, for example, on a P type semiconductor substrate, forming an N type impurity by ion implantation in the P type semiconductor substrate through a thin resist-free portion of said silicon oxide layer. A polycrystalline silicon layer is laminated. This polycrystalline silicon layer is selectively etched to provide a first wire. A thin silicon oxide layer set on the barrier regions is etched with the expected connection area of the first wire used as a mask. An N type impurity is again introduced by the ordinary diffusion or ion implantation process to form a deep barrier region around the expected connection area of the first wire. Later, a silicon oxide layer acting as a second insulation layer is superposed on the whole mass. Thereafter a contact hole is formed to expose the expected connection area of the first wire and part of the barrier regions. Last, a second wire is prepared from aluminium. This

second aluminium wire is connected to the expected connection area of a polycrystalline silicon wire through the contact hole and also to part of the barrier regions exposed around the expected connection area of the first wire.

The foregoing description refers to the case where the barrier regions surrounding the expected connection area were formed with a greater depth than the barrier regions lying below said expected connection area. Obviously, all the barrier regions may be formed with the same depth. The barrier regions surrounding the expected connection area of the first wire and those which lie below said expected connection area are made contiguous to each other. The first wire may be prepared from molybdenum or any other metal in place of polycrystalline silicon. The barrier regions are only required to have the opposite conductivity to that of the semiconductor substrate. Namely, the barrier regions may be P or N type, depending on the conductivity type of the semiconductor substrate.

Claims:

1. A semiconductor device having a semiconductor substrate of one conductivity type, first wire formed on a first insulation layer and a second wire connected to the expected connection area of the first wire through a contact hole of a second insulation layer, characterized in that barrier regions are formed on those portions of the surface of the semiconductor substrate which lie below and around the expected connection area of the first wire with the opposite conductivity type to that of the semiconductor substrate.

2. The semiconductor device according to claim 1, wherein the peripheral edges of the barrier regions are positioned below the second insulation layer on the outside of the contact hole.

3. The semiconductor device according to claim 1 or 2, wherein the barrier region surrounding the expected connection area of the first wire is formed with a greater depth than that which lies below said expected connection area.

4. The semiconductor device according to claim 1 or 2, wherein the barrier region surrounding the expected connection area of the first wire and that which is positioned below said expected connection area are formed with the same depth.

FIG. 1

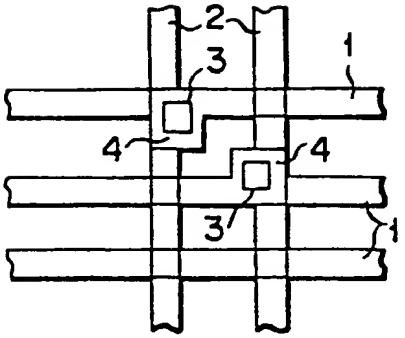

FIG. 2

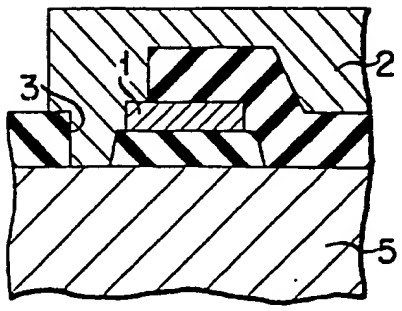

FIG. 3

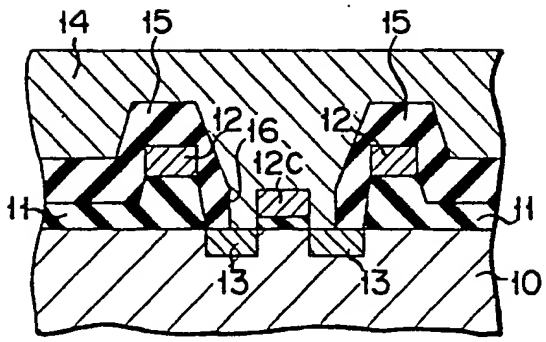

FIG. 4

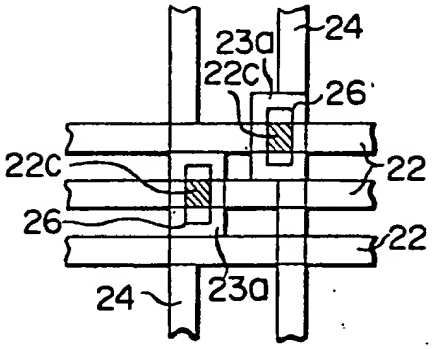

FIG. 5